Claims

[c1] 1. A method of adjusting process corners for adjusting timing of an integrated circuit design, said method comprising:

establishing initial voltage sensitivity curves relating to the relationship between gate timing variations caused by voltage supply changes and gate timing variations caused by manufacturing processing changes in a circuit design for slow and fast process extremes;

establishing an initial voltage supply at which initial process corners appear on said voltage sensitivity curves;

establishing revised process corners for which initial timing requirements are to be changed into revised timing requirements;

establishing revised voltage sensitivity curves relating to said revised process corners; and

changing said initial voltage supply to a revised voltage supply to accommodate said revised timing requirements based on where said revised process corners cross said revised voltage sensitivity curves.

[c2]   2. The method in claim 1, wherein said process of changing said initial voltage supply does not perform any of said manufacturing processing changes.

[c3]   3. The method in claim 1, wherein transistors in said circuit design are based on a common transistor design.

[c4]   4. The method in claim 1, wherein said revised timing requirements are used to determine whether manufactured chips are defective.

[c5]   5. The method in claim 1, wherein said initial timing requirements and said revised timing requirements comprise one of two extreme process corners for said circuit design consisting of either the fastest process timing allowed by said circuit design or the slowest process timing allowed by said circuit design.

[c6]   6. The method in claim 1, wherein said process of changing said initial voltage supply includes changing said initial voltage supply sufficiently to compensate for across chip line variation (ACLV).

[c7]   7. The method in claim 1, wherein said revised timing requirements comprise front end process timing requirements associated with said gate delay.

[c8]   8. A method of adjusting timing requirements of an inte-

grated circuit design, said method comprising:

establishing a circuit design having initial timing requirements and an initial voltage supply;

establishing a relationship between gate timing variations caused by voltage supply changes and gate timing variations caused by manufacturing processing changes;

changing said initial timing requirements to revised timing requirements; and

changing said initial voltage supply to a revised voltage supply to accommodate said revised timing requirements based on said relationship between gate timing variations caused by voltage supply changes and gate timing variations caused by manufacturing processing changes.

[c9] 9. The method in claim 8, wherein said process of changing said initial voltage supply does not perform any of said manufacturing processing changes.

[c10] 10. The method in claim 8, wherein said transistors in said circuit design are based on a common transistor design.

[c11] 11. The method in claim 8, wherein said revised timing requirements are used to determine whether manufactured chips are defective.

[c12]   12. The method in claim 8, wherein said initial timing requirements and said revised timing requirements comprise one of two extreme process corners for said circuit design consisting of either the fastest process timing allowed by said circuit design or the slowest process timing allowed by said circuit design.

[c13]   13. The method in claim 8, wherein said process of changing said initial voltage supply includes changing said initial voltage supply sufficiently to compensate for across chip line variation (ACLV).

[c14]   14. The method in claim 8, wherein said revised timing requirements comprise front end process timing requirements associated with said gate delay.

[c15]   15. A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method of changing timing requirements of an integrated circuit design, said method comprising:

establishing a circuit design having initial timing requirements and an initial voltage supply;
establishing a relationship between gate timing variations caused by voltage supply changes and gate timing variations caused by manufacturing process-

ing changes;

changing said initial timing requirements to revised timing requirements; and

changing said initial voltage supply to a revised voltage supply to accommodate said revised timing requirements based on said relationship between gate timing variations caused by voltage supply changes and gate timing variations caused by manufacturing processing changes.

[c16]   16. The program storage device in claim 15, wherein said process of changing said initial voltage supply does not perform any of said manufacturing processing changes.

[c17]   17. The program storage device in claim 15, wherein said transistor in said circuit design are based on a common transistor design.

[c18]   18. The program storage device in claim 15, wherein said revised timing requirements are used to determine whether manufactured chips are defective.

[c19]   19. The program storage device in claim 15, wherein said initial timing requirements and said revised timing requirements comprise one of two extreme process corners for said circuit design consisting of either the

fastest process timing allowed by said circuit design or the slowest process timing allowed by said circuit design.

[c20]   20. The program storage device in claim 15, wherein said process of changing said initial voltage supply includes changing said initial voltage supply sufficiently to compensate for across chip line variation (ACLV).